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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,379	04/20/2004	Eric R. Fossum	M4065.0628/P628-B	3781

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DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
PIZARRO CRESPO, MARCOS D	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/827,379	FOSSUM, ERIC R.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-37 and 40-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35-37 and 40-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Attorney's Docket Number: M4065.0628/P628-B

Filing Date: 4/20/2004

Claimed Priority Date: 8/29/2002 (Continuation of 10/230,079)

Applicant(s): Fossum

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on 12/8/2006.

Acknowledgment

1. The amendment filed on 12/8/2006, responding to the Office action mailed on 9/11/2006, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 35-37 and 40-50.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

3. **Claims 37, 41, and 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

4. Claim 37 recites the limitation "said stores" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Initially, and with respect to claims 37 and 42, note that a limitation in a claim with respect to the manner in which a claimed device is intended to be used does not differentiate the claimed device from a prior-art device if the prior-art device teaches all structural limitations in the claims and it is capable of performing the intended use. *In re Schreiber*, 28 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See *Hewlett-Packard Co. v. Bausch & Lomb Inc.* and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a device claim, and not the patentability of its functions (909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990)). As stated in Best,

> Where the claimed and prior art products are identical or substantially identical in structure or composition, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

7. **Note that the applicant has burden of proof** once the examiner establishes a sound basis for believing that the products of the applicant and the prior art are the same. See *In re Spada*, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990).

8. **Claims 35-37, 40, 42, 43, 45, 49, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao (US 6339248) in view of Kochi (US 6670990).**

9. Regarding claim 35, Zhao (see, *e.g.*, fig. 8) shows most aspects of the instant invention including a pixel comprising:

- ✓ A substrate **101**
- ✓ A photoconversion device fabricated in the substrate **101**
- ✓ A charge collection region **103** of the device
- ✓ A first conductivity type reset region **123** formed in the substrate **101**, coupled to the collection region **103**, and configured to apply a reset charge to the collection region in response to a pulsed reset signal applied to the reset region (see, *e.g.*, col.5/ll.30-34)
- ✓ A pulsed voltage source for providing said pulsed reset signal (see, *e.g.*, col.5/ll.30-34)

Zhao, however, fails to show a capacitor having a first terminal in electrical communication with the pulsed voltage source and a second terminal in electrical communication with the reset region. Kochi, on the other hand, teaches that said capacitor would allow changing the reset voltage of Zhao so as to let the source follower operate linearly (see, *e.g.*, Kochi: col.16/lll.13-15). Thus, avoiding deterioration of the input-output linearity in the low luminosity region and widening the dynamic range to obtain image signals of a higher source/noise ratio (see, *e.g.*, Kochi: col.1/ll.40-45 and col.3/ll.1-10).

It would have been obvious at the time of the invention to one of ordinary skill in the art to incorporate in Zhao's pixel cell a capacitor having a first terminal in electrical communication with the pulsed voltage source and a second terminal in electrical

communication with the reset region, as suggested by Kochi, to widen the dynamic range of the pixel and obtain image signals of a higher source/noise ratio.

10. Regarding claim 36, Zhao shows the reset region **123** and the collection region **103** both forming an extended charge collection region (see, *e.g.*, fig. 8), the extended charge collection region also being reset by the pulsed reset signal (see, *e.g.*, col.5/ll.30-34).

11. Regarding claim 37, Zhao shows most aspects of the instant invention (see, *e.g.*, paragraphs 6 and 7 above) including:

- ✓ A source follower transistor **151** for outputting a signal representing charge collected in the extended collection region
- ✓ A row select transistor **153** for selectively outputting a signal from the source follower transistor **151**

12. In reference to the language in claim 37 referring to the function of the capacitor, it is noted that Zhao/Kochi show all aspects of the semiconductor device according to the claimed invention (see paragraphs 9-11 above) and that using the capacitor to store charge collected in the collection region is a function that does not affect the structure of the final device. Furthermore, Zhao/Kochi's device is capable of performing the claimed functions. For example, if, as suggested by their combination, the first capacitor plate of Kochi were connected to the photodiode of Zhao, then applying a high voltage **V2** to the second plate would result in carriers generated at the photodiode easily flowing into the n-doped region **123** and being stored at the capacitor **1101** (see, *e.g.*, Zhao/fig.8 and Kochi/fig.14).

13. Regarding claim 40, Zhao shows the first conductivity type is n-type.

14. Regarding claim 42, Zhao (see, *e.g.*, fig. 8) shows most aspects of the instant invention including a pixel for use in an imaging device, the pixel consisting essentially of:

- ✓ A charge collection region **103** provided in a substrate
- ✓ A reset region **123** in the substrate adjacent to the charge collection region **103** for periodically resetting a charge level of the collection region **103** in response to a reset signal applied to the reset region (see, *e.g.*, col.5/ll.30-34)
- ✓ A source follower transistor **151** for outputting a signal representing charge collected in the collection region **103**
- ✓ A row select transistor **153** for selectively outputting a signal from the source follower transistor **151**
- ✓ A pulsed voltage source for providing the reset signal to the reset region (see, *e.g.*, col.5/ll.30-34)

Zhao also shows the source follower transistor **151** in electrical communication with the reset region **123**, but fails to show a capacitor in electrical communication with the reset region **123** and the source follower transistor **151** for storing charge collected in the collection region.

Kochi, on the other hand, teaches that said capacitor would allow changing the reset voltage so that the source follower of Zhao would operate linearly (see, *e.g.*, Kochi: col.16/ll.13-15). This would avoid deteriorating the input-output linearity in the

low luminosity region and would allow widening the dynamic range to obtain image signals of a higher source/noise ratio (see, *e.g.*, Kochi: col.1/ll.40-42 and col.3/ll.1-10).

It would have been obvious at the time of the invention to one of ordinary skill in the art to incorporate in Zhao's pixel a capacitor having a first terminal in electrical communication with the pulsed voltage source and a second terminal in electrical communication with the reset region, as suggested by Kochi, to widen the dynamic range of the pixel and obtain image signals of a higher source/noise ratio.

15. In reference to the language in claim 42 referring to the function of the capacitor, see the comments above in paragraph 12, which comments are considered repeated here.

16. Regarding claim 43, Zhao shows the reset region **123** and the collection region **103** both forming an extended charge collection region (see, *e.g.*, fig. 8). Zhao also shows (see, *e.g.*, col.5/ll.30-34) a voltage source periodically supplying the reset signal.

17. Regarding claim 45, Zhao shows the reset region **123** is doped with an n-type dopant at a first dopant concentration (see, *e.g.*, fig. 8).

18. Regarding claims 49 and 50, Kochi teaches that the charge level of the charge collection region is resetted before and after charge is collected in the collection region (see, e.g., col.2/ll.18-20, col.3/ll.42-45, col.8/ll.35-38, and col.15/ll.58-62).

19. **Claims 41 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao/Kochi in view Dasgupta (US 6146939).**

20. Regarding claims 41 and 44, Zhao/Kochi show most aspects of the instant invention including a capacitor in electrical communication with the reset region and the source follower transistor (see, *e.g.*, paragraphs 9 and 14 above). As taught by

Dasgupta, every capacitor has a capacitance per unit area associated with it. This capacitance may range from 4.3-5.3 $fF/\mu m^2$ depending on the choice and thickness of the capacitor dielectric (see, *e.g.*, Dasgupta, col.1/ll.37 and col.3/ll.13-19). Zhao/Kochi, however, fail to specify that the capacitance per unit area of the capacitor is between about 5-10 $fF/\mu m^2$. However, these capacitance values will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such values are critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

Since the applicant has not established the criticality (see next paragraph) of the claimed capacitance values, and since these values are in common use in similar capacitors in the art, as taught by Dasgupta, it would have been obvious to one of ordinary skill in the art to use these values in the device of Zhao/Kochi.

CRITICALITY

21. The specification contains no disclosure of either the critical nature of the claimed capacitance or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

22. **Claims 46-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao/Kochi in view of Wada (US 6677676).**

23. Regarding claims 46-48, Zhao/Kochi shows most aspects of the instant invention (see, *e.g.*, paragraphs 14 and 17 above). They, however, fail to show the region where the capacitor contacts the reset region having a higher concentration than the reset region. Wada, on the other hand, teaches that doing so would establish a good

electrical connection between the capacitor and the reset region (see, *e.g.*, Wada: col.12/ll.28-31).

It would have been obvious at the time of the invention to have Zhao/Kochi's contact region having a higher concentration than the reset region, as suggested by Wada, to establish a good electrical connection between the capacitor and the reset region.

Response to Arguments

24. The applicant argues:

> Claims 35 recites that the capacitor has a first terminal connected to the pulsed voltage source and a second terminal connected to the reset region. Claim 42 recites that the capacitor is in electrical communication with the pulsed voltage source, the reset region, and the source-follower transistor. Koichi, on the other hand, teaches a first capacitor **1101** formed between the reset switch **114** and the gate of the MOS transistor **102** (see, *e.g.*, col.15/ll.51-53). MOS transistor **102** is a row-select transistor, not a source-follower transistor. Koichi further teaches that capacitor **1102** is formed between the gate of the MOS transistor and ground (see, *e.g.*, col.15/ll.55-57). Therefore, capacitors **1101** and **1102** cannot read on the capacitor of the claimed invention.

25. The examiner responds:

Firstly, Kochi's MOS transistor **102** is a source-follower transistor and not a row-select transistor as the applicant indicated (see, *e.g.*, col.8/ll.7-8). Lastly, Koichi clearly shows the capacitor **1101** having a first terminal connected to the voltage source **V2** and a second terminal connected to the reset region **114**, as recited in claim 35. He also shows the capacitor in electrical communication with the voltage source **V2**, the reset region **114**, and the source-follower transistor **102/103**, as recited in claim 42.

26. The applicant argues:

> Zhao (see, *e.g.*, col.3/ll.67-col.4.ll.3) discloses that "the P+ region...is not connected to the Pwell or Psub layers, thus making the P+ region floating. This avoids the addition of extra capacitance to the cell." Therefore, Zhao teaches away from the use of a capacitor.

27. The examiner responds:

Contrary to applicant's assertions, Zhao does not teach against adding a capacitor to the cell. Every pixel cell having a photodiode and transistors will have associated therewith an inherent parasitic capacitance. This capacitance is an inevitable property of every pixel cell (see, *e.g.*, Hosier: col.5/ll.25-35). It is caused by the relative proximity of the photodiode, the transistors, and the wires interconnecting these cell parts (see, *e.g.*, Takebe: col.1/ll.50-55, and Sakai: col.4/ll.20-40). In this context, Zhao teaches that the contribution to the parasitic capacitance that a pinned photodiode would have as a result of the P+ reset region being connected to the Psub and Pwell is not formed in his pixel cell because the P+ reset region is floating. Or as he says in the abstract, there is no extra capacitance added to the cell (see, *e.g.*, Zhao: abstract/col.5-10).

Applicant's comments, however, seem to imply that Zhao teaches against having a capacitor in the pixel cell and this is clearly not the case. Although he teaches that his design avoids adding an extra capacitance to the cell, he never teaches that there would be any deleterious effects from having that extra capacitance nor does he teach against Kochi's capacitor being added to Zhao's cell. In fact, Kochi even teaches that his capacitance may be provided either by an intentionally formed capacitor or by using the very same parasitic capacitance of the cell, which is inherent to the cell (see, e.g., Kochi: col.15/ll.53-55).

Conclusion

28. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 10:00 AM to 8:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

30. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the

automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

31. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/59,72,222,223,225,228-234,290-294,431-466	2/21/7
Other Documentation: PLUS Analysis	8/15/05
Electronic Database(s): EAST (USPAT, EPO, JPO)	2/21/7

Marcos D. Pizarro-Crespo
Primary Examiner
Art Unit 2814
571-272-1716
marcos.pizarro@uspto.gov

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